REMARKS/ARGUMENTS

Claims 1-17 are pending in the application.

Claims 1-4 and 6-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,526,481 to Shen et al. in view of U.S. Patent 6,859,861 to Rhodes.

The Examiner has agreed that Shen fails to disclose a plurality of sub-unit caches recited in claims of the present application. However, the Examiner has asserted that it is well known in the cache art to divide a cache into a plurality of sub-unit caches, referring to Rhodes. Applicants respectfully disagree.

1. Shen is Improper §103(a) Prior Art

The claimed invention is about cache-coherent *input/output* device, but Shen is about adaptive cache coherence protocols for *multiple processors*. As discussed in the background section of the present application, I/O devices are non-cacheable devices, but processors are cacheable devices. Shen is irrelevant to the claimed invention.

As shown in Figs. 1 and 2 of Shen, the shared memory system of Shen provides a cache 130 for each instruction processor 110. Shen incorporates adaptation or selection of cache protocols during operation while guaranteeing semantically correct processing of memory instructions *by multiple processors* (Shen, col. 3, lines 26-30).

However, as discussed in the background section of the present application, it is known that multiple cache systems have been utilized in multi-processor computer system designs, a

coherency protocol is implemented to ensure that each processor retrieves only the most up-to-date version of data from the cache, and processors are commonly referred to as "*cacheable*" devices. However, I/O components, such as those coupled to a Peripheral Component Interconnect Bus, are generally *non-cacheable* device. A purpose of embodiments of the present application is to improve performance of I/O devices (Specification, page 3, the first and second full paragraphs).

In short, the claimed invention is about input/output devices, which are non-cacheable devices. But Shen is about a shared-memory system for multi-processors, which are cacheable devices. Thus, Shen is irrelevant to the purpose of the claimed invention, and is improper §103(a) prior art.

2. It is Improper to Reconstruct the Claimed Invention with Shen and Rhodes.

Claims of the present application recite a cache-coherent *input/output device*.

As discussed above, Shen is irrelevant to the claimed cache-coherent input/output device.

Rhodes is irrelevant to a cache-coherent input/output device as well. According to Rhodes, although cache memories have been particularly arranged in the prior art to expedite computer operations, the ever increasing *speed of processors* renders it desirable to further improve memory arrangements for expediting computer operations (Rhodes, col. 1, lines 27-31).

Thus, Shen and Rhodes concern memory for *processors*, but the claimed invention recites a cache-coherent *input/output device*. Since the problems solved by Shen and Rhodes are very

different from recited elements of the claimed invention, there is no suggestion or motivation to combine Shen and Rhodes to reconstruct the claimed invention.

3. The Cited References Fail to Teach the Claimed Cache Coherent Input/Output Device.

Even assuming, *arguendo*, that a skilled artisan were to combine Shen and Rhodes, the combination would not result in the claimed invention, since neither Shen nor Rhodes discloses the claimed cache coherent input/output device..

The Examiner has argued that Shen discloses a cache-coherent I/O device, referring to element 110 in Fig. 2 of Shen. However, elements 110 of Shen are instruction processors, not I/O devices.

The Examiner has argued that Applicants state in the present application that "an input/output device may be utilized as a caching I/O device" is well known in the memory art. However, according to the sentence immediately following the statement cited by the Examiner, in the prior art, when an input/output device is used as a caching I/O device, the I/O device includes a single, monolithic caching resource for data. The prior art fails to teach or suggest a cache-coherent I/O device having a plurality of sub-unit caches.

The Examiner has argued that, according to the present application, "a cache coherency protocol" is well known in the memory art to synchronize data in a plurality of caches. However, that statement is about cache systems for multi-processors in a computer system, instead of I/O devices.

Rhodes discloses cache memory structures for alleviating the continually increasing memory latency or delay problem caused by the ever increasing speed of *computer processors* (Rhodes, Abstract). Thus, Rhodes fails to disclose a cache-coherent input/output device.

Accordingly, the prior art fails to teach or suggest the claimed cache-coherent input/output device. Applicants respectfully submit that claims 1-17 are patentable over the combination of Shen and Rhodes.

Claims 5, 13 and 15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shen in view of Rhodes and further in view of Jim Handy, "The Cache Memory Handbook", TK7895.M4H35, 1993, pp 140-240.

Handy discloses a protocol for use in *multiple processor system* with multiple caches. Handy fails to teach a cache-coherent input/output device, and does not supply any deficiency of Shen or Rhodes. Accordingly, Applicants respectfully submit that claims 5, 13 and 15 are patentable over the combination Shen, Rhodes and Handy for this additional reason as well.

Claims 16 and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Shen in view of Rhodes and Handy, and further in view of Witt et al. (U.S. Patent 6,202,139).

Witt discloses a computer system including a processor having a cache which includes multiple ports. The cache is pipelined and operates at a clock frequency higher than that employed by the remainder of the microprocessor including the cache for multiple accesses per clock cycle (Witt, col. 2, lines 31-36 and Abstract). Thus, Witt fails to teach a cache-coherent input/output device and does not supply any deficiency of Shen, Rhodes, or Handy.

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Accordingly, Applicants respectfully submit that claims 16 and 17 are patentable over the combination of Shen, Rhodes, Handy and Witt.

For all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited. The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to the deposit account of Kenyon & Kenyon LLP , deposit account no. **11-0600.**

Respectfully submitted,

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